

Customer No.: 31561
Application No.: 10/711,535
Docket No.: 11041-US-PA-1

REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 1-11. The Office Action rejected claims 1-6 and 8-11 under 35 U.S.C. 102(e) as being anticipated by Lee (U.S. 6,444,525) (hereinafter Lee).

The Office Action rejected claim 7 under 35 U.S.C. 103(a) as being unpatentable over Lee.

Applicants submit that independent claim 1 and dependent claim 9 have been amended, dependent claim 8 have been canceled while the other claims remain unchanged as originally filed. All changes to the claims are fully supported by the originally filed claims, disclosure and the drawings. For at least the following reasons, Applicant respectfully submits that claims 1-11 are in proper condition for allowance. Reconsideration is respectfully requested.

Discussion of the claim rejection under 35 USC 102(e)

Claims 1-6 and 8-11 were rejected under 35 U.S.C. 102(e) as being anticipated by Lee '525.

In response to the rejections thereto, Applicants have amended claim 1, and hereby otherwise traverse these rejections for at least the reasons set forth below. As such, Applicants submit that method, as set forth in claim 1 is novel and unobvious over Lee '525, or any of the other cited references, taken alone or in combination, and thus

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should be allowed.

With respect to claim 1, as amended, recites in parts:

A method of fabricating a flash memory cell, comprising the following steps:

...forming a conformal conductive layer on the substrate;
performing anisotropic etching to the conformal
conductive layer to form a first conductive spacer on a
sidewall of the first opening as a select gate and a second
conductive spacer on a sidewall of the second opening as a
floating gate simultaneously;

... (Emphasis added)

Applicants submit that Lee '525 failed to teach, suggest, or disclose, a method comprising "forming a conformal conductive layer on the substrate; and performing anisotropic etching to the conformal conductive layer to form a first conductive spacer on a sidewall of the first opening as a select gate and a second conductive spacer on a sidewall of the second opening as a floating gate simultaneously", as required by claim 1. Addressing the above limitation, the Examiner designated Fig. 2L (9a and 9b), and also Fig. 2M (12a). However, Lee '525 clearly teaches: "the floating gate 9a is formed at the sidewall of the first trench 3, and the gate 9b of the select transistor may be formed at the sidewall of the second trench 5" (col. 3, lines 45-47). As also alleged by the Examiner addressing claim 1, the first trench 3 and the second trench 5 read on the first opening and

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the second opening, respectively. As such, as interpreted by the Examiner in accordance with Lee '525, formed on the first opening is the floating gate 9a, rather than a "select gate" as required by claim 1, and formed on the second opening is the gate 9b of a select transistor, rather than a "floating gate" as required by claim 1.

Furthermore, Applicants submit that it should be understood by those of ordinary skill in the art, item 6a of Lee '525 is indeed the spacer structure employed therein. However, such a spacer 6a is dielectric layer rather than a conductive spacer, and thus cannot be used to read on this specified claimed subject matter, i.e., first and second conductive spacers, as well.

Furthermore, in forming conductive spacers, the present method as set forth in claim 1, requires only a single etching process. However, as taught by Lee '525, items 9a and 9b are configured by two individual etching processes (FIGS. 2H-2J). This provides further evidence showing that 9a and 9b are not spacers understood by those of ordinary skill in the art at all.

For failing to teach each and every limitation of claim 1, Lee '525, does not *prima facie* anticipate the claimed invention, as set forth in claim 1 and its dependent claims 2-6, and 9-11. Claims 2-6, and 9-11 are therefore submitted to be novel and unobvious over Lee '525, or any of the other cited references, taken alone or in combination, and thus should be allowed.

Discussion of the claim rejection under 35 USC 103(a)

Claim 7, 10, 13 was rejected under 35 U.S.C. 103(a) as being unpatentable over

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Lee '525.

In response to the rejections thcreto, Applicants submit that claim 7 depend on allowable claim 1, and thus should also be allowable.

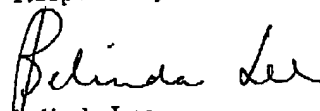
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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-11 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,


Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jicigroup.com.tw
Usa@jicigroup.com.tw